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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,095	09/23/2003	Michael R. Butts	706316-1224	1861

7590 11/02/2005

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 11/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,095	BUTTS, MICHAEL R.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/669,095 filed 09/23/2003.

2. Claims 1-22 are pending in the Application.

Claim Objections

3. Claims 10-13 and 18-22 are objected to because of the following informalities:

Claims 10-13 and 18-22 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoare et al. (US Patent Application Publication 20020133325).

With respect to claim 1 Hoare et al. teaches a design verification system for verifying functionality of electronic designs within the method and system for the

functional verification of the circuit design (abstract; paragraph [0103]), comprising: at least one programmable logic device, the programmable logic device comprising a plurality of logic elements that can be placed in electrical communication with one another within PLD such as FPGA containing plurality of connected logic elements (paragraphs [0102], [0103]); at least one logic processor programmed into the programmable logic device, the at least one logic processor utilizing at least one of the plurality of logic elements of the programmable logic device, the at least one logic processor comprising a logic functional unit that executes Boolean instructions within hardware accelerators (processors) (paragraph [0097]) which utilize FPGAs (paragraph [0102]) as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein the Boolean instruction is one of the plurality events might be simulated (abstract); at least one macro processor programmed into the programmable logic device, the at least one macro processor utilizing at least one of the plurality of logic elements of the programmable logic device, the at least one macro processor comprising a macro functional unit that executes macro instructions as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041]); and an interconnect architecture programmed into the programmable logic device, the interconnect architecture placing each of the at least one logic processor and the at least one macro processor in

communication with every other of the at least one logic processor and the at least one macro processor within the simulation engine including netlist containing primitive logic gates and connectivity information between them (paragraphs [0084], [0117]).

With respect to claim 8 Hoare et al. teaches a method for implementing a design verification system into at least one programmable logic device so that a user design to be verified can be implemented therein within the method and system for the functional verification of the circuit design (abstract; paragraph [0103]), comprising: mapping the user design into operations for execution within a central scheduler to evaluate discrete events including discrete event simulation engines (processors) including mapping different types of simulation engines (processors) to multiple components of the discrete event system (paragraphs [0065], [0034], [0067]); partitioning each of the operations into processor types suitable for each of the operations within dividing the netlist into subgroups of components based on the type of the simulation engine that will be used to evaluate the component (paragraph [0067]); ordering each of the processor types according to connectivity of each of the processor types within the central scheduler to sort and schedule executing discrete events sequentially (paragraph [0034]); scheduling communications between each of the processor types within direct input and output queues between the scheduler and each of the simulation engines (Paragraph [0035]); and programming each of the at least one programmable logic device with each of the processor types within the emulation process including mapping the gate level design into a reconfigurable architecture (PLD) for programming the netlist (paragraphs [0080], [0102]).

With respect to claim 17 Hoare et al. teaches a method for verifying functionality of an electronic design within the method and system for the functional verification of the circuit design (abstract; paragraph [0103]), the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit as shown on the Fig. 6 (abstract; paragraph [0108]), comprising; compiling the electronic design into logic processors that execute the Boolean logic gates (abstract), at least one macro processor that executes the at least one macro function, at least one memory processor that executes the at least one memory circuit as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041]); and an interconnect architecture that interconnects the logic processors, the at least one macro processor and the at least one memory processor to one another as shown on the Fig. 6 as combination of the multiple simulation engines, wherein the combination might be in different various (paragraphs [0041]; [0108]); programming the logic processors, the at least one macro processor and the at least one memory processor into at least one programmable logic device hardware logic emulators having ability utilizing the PLD (paragraph [0102]); applying stimulus to the logic processors programmed into the at least one programmable logic device, the at least one macro processor programmed into the at least one programmable logic device and the at least one memory processor programmed into the at least one programmable logic device such that the logic

processors execute the Boolean logic gates, the at least one macro processor executes the at least one macro function and the at least one memory processor executes the at least one memory circuit within hardware accelerators (processors) (paragraph [0097]) which utilize FPGAs (paragraph [0102]) as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein the Boolean instruction is one of the plurality events might be simulated (abstract), wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041]); and collecting output responses generated by the logic processors programmed into the at least one programmable logic device, the at least one macro processor programmed into the at least one programmable logic device and the at least one memory processor programmed into the at least one programmable logic device within the method and system for verifying the integrated circuit design using hardware emulator (accelerator), which utilize FPGA, wherein FPGAs enable processor-based (hardware) emulator as described above, including the scheduler and simulation engines for collecting the results of the verification process (abstract; paragraph [0069]).

With respect to claims 2-7, 9-16 and 18-22 Hoare et al. teaches:

Claims 2, 19: at least one memory processor programmed into the programmable logic device, the at least one memory processor comprising a memory functional unit that can store data, the at least one memory processor in communication with the at least one logic processor and the at least one macro processor through the

interconnect architecture as shown on the Fig. 6 depicting the discrete event logic simulation system including memory and CAMs engine (paragraph [0108]);

Claims 3, 10: at least one memory processor comprises: an instruction memory; a register file controlled by the instruction memory within macro block (logic) engine including logic memory for execution instructions (paragraph [0032]), the register file having outputs selectively in communication the memory functional unit, the register file comprised of input registers and local registers, the input registers in communication with the interconnect architecture, the local registers in communication with output from the memory functional unit (paragraphs [0170]-[0172]);

Claims 4, 18: the interconnect architecture comprises: an instruction memory within the fourth simulation engine as the interconnection and netlist simulation engine (paragraphs [0117], [0118]); a plurality of buffers, wherein the number of the plurality buffers is equal to the sum of the number of the at least one logic processor added to the number of the at least one macro processor added to the number of the at least one memory processor, each of the plurality of buffers having an output that is selected by the instruction memory the pending and future event queues (PEQ and FEG which plat a role of the buffers that temporarily hold the vents until evaluation or scheduling (paragraph [0125]); a plurality of selectors, wherein the number of the plurality of selectors is equal to the number of the plurality of buffers, each of the plurality of selectors in communication with each of the plurality of buffers so that data stored in any of the plurality of buffers can be transmitted to any of the plurality of selectors, each of the plurality of selectors controlled by the instruction memory; and a plurality of output

ports, each of the plurality of output ports corresponding to one of the plurality of selectors the scheduler manager to sort and manage PEQ and FEQ (paragraph [0133]);

Claims 5, 11, 20: a general purpose processor, the general purpose processor comprising a central processing unit that executes computer instructions, the general purpose processor in communication with the at least one logic processor and the at least one macro processor through the interconnect architecture (paragraph [0031]);

Claims 6, 12, 21: the logic processor comprises: an instruction memory macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]); a register file controlled by the instruction memory, the register file having outputs selectively in communication with the logic functional unit, the register file comprised of input registers and local registers, the input registers in communication with the interconnect architecture, the local registers in communication with output from the logic functional unit within macro block (logic) engine (paragraphs [0108], [0111]), wherein might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041], [0170]-[0172]);

Claims 7, 13, 22: the macro processor comprises: an instruction memory wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]); and a register file controlled by the instruction memory, the register file having outputs selectively in communication the macro functional unit, the register file comprised of input registers and local registers, the input registers in communication with the interconnect architecture, the local registers in communication with output from the macro functional unit within macro block (logic) engine (paragraphs [0108], [0111]),

wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041], [0170]-[0172]);

Claim 9: the processor types comprise logic processors, macro processors, memory processors and general purpose processors within different types of simulation engines described above and (paragraph [0031]);

Claim 14: the partitioning step comprises: consulting a programmable logic device library that has a preprogrammed mix of said processor types within dividing the netlist into subgroups of components based on the type of the simulation engine that will be used to evaluate the component (paragraph [0067]); and selecting an appropriate preprogrammed mix of said processor types for said operations for execution within the central scheduler to sort and schedule executing discrete events sequentially (paragraph [0034]) including direct input and output queues between the scheduler and each of the simulation engines (Paragraph [0035]);

Claim 15: scheduling step comprises: creating a program for instruction memories within each of said processor types as shown on the Fig. 3 (paragraph [0079]); and creating programming files for each programmable logic device used for verifying the user design (paragraphs [0084], [0085]);

Claim 16: loading the program into each of the instruction memories (paragraph [0085]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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